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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/592,449	06/12/2000	William C. Moyer	SC11119TH	7033

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,449	MOYER ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/12/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on ___ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2/3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: At page 12, line 29, "abodiments" should read --embodiments--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2-5 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, lines 6-9, it is not clear whether the "control circuitry" is the element of the "instruction fetch unit". Note in Fig. 2, the "control circuitry" (216) is one of the elements inside the "instruction fetch unit" (220). However, the "control circuitry" is claimed as an independent element. Similar problems exist in the other claim 13.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 7-13, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Great Britain Patent No. 2,283,595 (Herein referred as GB'595).

Referring to claim 1, GB'595 discloses, as claimed, a data processing system having a first and a second mode of operation, comprising: a central processing unit (10 see Fig. 3) having a first input to receive a first signal (the bits from the "Branch Instruction" data path received by the branch prediction logic unit 70 (see page 15, lines 17-20) is interpreted as the first signal in the static-branch-with-BHT-update mode) wherein a first state (the second state of the single taken/not-taken bit, see page 15, lines 33-35, and page 16, line 1) of the first

signal enables the first mode of operation and a second state (the first state of the single taken/not-taken bit, see page 15, lines 30-33) of the first signal enables the second mode of operation, wherein: the first mode of operation utilizes branch prediction (since the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1); and the second mode of operation utilizes substantially no branch prediction (since the address generated by sequential address calculator 72 is selected, see page 15, lines 30-33).

Referring to claims 2 and 13, GB'595 also discloses: the selecting circuitry (MUX 68, see Fig. 3) having a first input for receiving a sequential address (from sequential address calculator 72, see Fig. 3), a second input for receiving a target address (from branch address calculator 74, see Fig. 3), and a third input for receiving a control signal (from branch prediction logic unit 70, see Fig. 3) to select between the first input and the second input, and an output for providing one of the first input and the second input (see Fig. 3); an instruction fetch unit(comprising sequential address calculator 72 and branch address calculator 74), coupled to the selecting circuitry (MUX 68, see Fig. 3), having a first output to provide the sequential address(from sequential address calculator 72,

see Fig. 3) and a second output for providing the target address (from branch address calculator 74, see Fig. 3); and control circuitry (branch prediction logic unit 70, see Fig. 3), coupled to the selecting circuitry, having a first input to receive the first signal (mode bits, see Fig. 3) and having a first output (the output to MUX 68, see Fig. 3) to provide the control signal based on the first signal.

As to claims 7 and 15, GB'595 also discloses: a control register having a field corresponding to the first signal, wherein the field is capable of being dynamically programmed (as set forth above, the first signal is from the bits from the "Branch Instruction" data path received by the branch prediction logic unit 70 (see page 15, lines 17-20) is interpreted as the first signal in the static-branch-with-BHT-update mode, the signal inherently can temporarily stored in a control register, such as instruction register, in the system during the data movement).

As to claim 8, GB'595 also discloses: the data processing system(10, see Fig. 1) comprising only the central processing unit (10).

As to claim 9, GB'595 also discloses: the first mode of operation results in a first address setup timing; and the

second mode of operation results in a second address setup timing, wherein the first address setup timing allows for an earlier address valid time as compared to the second address setup timing (since the first mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1) .

Referring to claim 10, GB'595 discloses, as claimed, a data processing system having a first and a second mode of operation, comprising: a first input to receive a first signal (the bits from the "Branch Instruction" data path received by the branch prediction logic unit 70 (see page 15, lines 17-20) is interpreted as the first signal in the static-branch-with-BHT-update mode) wherein a first state (the first state of the single taken/not-taken bit, see page 15, lines 30-33) of the first signal enables the first mode of operation and a second state (the second state of the single taken/not-taken bit, see page 15, lines 33-35, and page 16, line 1) of the first signal enables the second mode of operation, wherein: the first mode of operation results in a first address setup timing; and the second mode of operation results in a second address setup timing that allows for an earlier address valid time as compared

to the first address setup timing (since the second mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1).

Referring to claim 11, GB'595 discloses: the first address setup timing is realized utilizing a first level of branch prediction, and the second address setup timing is realized utilizing a second level of branch prediction that is more aggressive than the first level of branch prediction (as set forth above, the second mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1)..

Referring to claims 12 and 19, GB'595 discloses: the first mode of operation performs substantially no branch predictions (the address generated by sequential address calculator 72 is selected, see page 15, lines 30-33).

Referring to claim 16, GB'595 discloses, as claimed, in a data processing system having a first and a second mode of operation, a method for altering an address setup time

comprising: receiving a first input signal (the bits from the "Branch Instruction" data path received by the branch prediction logic unit 70 (see page 15, lines 17-20) is also interpreted as the first signal in the static-branch-with-BHT-update mode); if the first input signal has a first state(the first state of the single taken/not-taken bit, see page 15, lines 30-33), operating in the first mode of operation, wherein the first mode of operation results in a first address setup timing; if the first input signal has a second state(the second state of the single taken/not-taken bit, see page 15, lines 33-35, and page 16, line 1), operating in the second mode of operation, wherein the second mode of operation results in a second address setup timing having an earlier address valid time as compared to the first address setup timing (since the second mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1)..

As to claim 17, GB'595 also discloses: the first mode of operation utilizes a first level of branch prediction and the second mode of operation utilizes a second level of branch prediction (since the second mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses

the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1; and also note the first mode of operation uses not taken prediction).

As to claims 18 and 20, GB'595 also discloses: the first level is less aggressive than the second level; and operating in the first mode of operation comprises resolving a condition of a branch instruction prior to accessing a target instruction of the branch instruction (as set forth above, the second mode of operation utilizes branch prediction at the earlier time, see page 5, line 15, and uses the address generated by branch address calculator 74 is selected, see page 15, line 35, and page 16, line 1; and also note the first mode of operation uses not taken prediction).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over GB'595.

GB'595 discloses the claimed invention except for: the first signal being hardwired to a predetermined state.

However, using a signal being hardwired to a predetermined state to speed up the signal process is old and well known in the art.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify GB'595's system to comprise the first signal being hardwired to a predetermined state, in order to speed up the signal process for the GB'595's system.

Allowable Subject Matter

8. Claims 3-5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: GB'595 is the closest reference. However, GB'595 does not teach or fairly suggest a data

processing system comprising: the control circuitry having a second input to receive a condition signal and a third input to receive a branch decode signal, and the control signal being based further in part on the condition signal and the branch decode signal.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references, such as Potter et al.'307; Ando'294; and Krishanan et al.'197 also taught limitations as claimed.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to

the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

12. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:**

Official faxes: 703-746-7239; and

After Final faxes: 703-746-7238.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
June 30, 2003